REMARKS

I. Interview Summary

Applicant thanks the Examiner for the courtesy of a telephone interview on June 6, 2006. The conversation focused on the fact that the prior art of record is directed toward dynamic debugging processes. In contrast, the present invention is directed toward post-processing operations that are performed after a task is executed. Amendments and arguments to more fully explore these issues are presented herewith.

II. 35. U.S.C. 101 Rejection

Claim 24 is rejected under 35 U.S.C. 101. Claim 24 is canceled, without prejudice, to expedite prosecution.

III. Prior Art Rejections

The claims are rejected in view of ALPERT (U.S. Patent 5,621,886), a MIPS reference (MIPS64 5Kc™ Processor Core Datasheet), and LINDSEY (U.S. Patent 5,870,606). The independent claims are amended to more fully distinguish over the prior art of record. Reconsideration of the rejection in view of the foregoing amendments and the following remarks is respectfully requested.

Independent claim 1 is amended to recite the operation of "retrieving said trace information..." Support for this amendment may be found in paragraph [1022] among other places.

Independent claim 1 is also amended to recite that the trace information is retrieved "with post-processing trace regeneration software operative to reconstruct said trace information." Support for this amendment may be found in paragraph [1022] and in the original claim language.

The foregoing amendments fully distinguish claim 1 over the prior art of record. In particular, the foregoing amendments make clear that the trace information is not part of a dynamic debugging process. Instead, the trace information is processed "after said task is

executed" using "post-processing trace regeneration software". This information is retrieved for the purpose of reconstructing trace information. A dynamic process does not involve "post-processing". A dynamic process uses the information currently available; a dynamic process does not retrieve trace information and then reconstruct that trace information, as claimed.

The MIPS reference describes JTAG Debug Support, which is a dynamic or interactive operation performed by a user. In other words, a user dynamically works in a debug mode. Thus, there is no trace memory, since all operations are performed dynamically. In addition, there is no need to transmit synchronization information including processor mode values and ASID values to a trace memory since all debugging is performed in a dynamic mode. Thus, the MIPS reference fails to show or suggest the limitations of claim 1.

Similarly, ALPERT discloses dynamic or interactive debug operations. For example, ALPERT states at column 5, lines 1-6: "This document describes an invention allowing for the separate enablement of debug events during the execution of operating system routines and non-operating system routines. This allows programmers the flexibility of selectively enabling debug events during the execution of either handlers, or applications, or both." ALPERT performs debug operations while a current process is suspended (see, for example, Figure 2).

Thus, ALPERT is a dynamic system with no need for a trace memory. Since ALPERT operates dynamically and does not have a trace memory, the patent does not show or suggest transmitting "to said trace memory synchronization information including processor mode values and ASID values", as currently claimed.

Even if ALPERT's registers are considered to be a trace memory, ALPERT does not show or suggest retrieving trace information after the task is executed with post-processing trace regeneration software operative to reconstruct trace information, as claimed. Accordingly, ALPERT fails to show or suggest the limitations of amended claim 1.

The Examiner points to LINDSEY for teaching that trace information can be utilized after execution of a task. The sections of LINDSEY cited by the Examiner do not have any concrete information on how or when tracing is accomplished. LINDSEY provides no information on synchronization of trace information. MIPS and ALPERT do not address the issue of synchronizing trace information, because they are operative in a dynamic mode, where such synchronization is not required. Thus, the combination of LINDSEY, MIPS and ALPERT fail to show or suggest the claimed invention. In particular, the references fail to show or

suggest transmitting to said trace memory synchronization information including processor mode values and ASID values and then retrieving the trace information after a task is executed with post-processing trace regeneration software operative to reconstruct the trace information, as currently claimed.

In sum, MIPS, ALPERT, and LINDSEY individually and in combination fail to show or suggest the limitations of amended claim 1. Therefore, claim 1 should be in a condition for allowance. Claims 3, 5-6, and 10 are dependent upon claim 1 and therefore should also be in a condition for allowance. Claim 10 includes a number of limitations that are not shown or suggested by the prior art of record.

The remaining independent claims are amended to include limitations of the type incorporated into claim 1. Thus, each patentability argument with respect to claim 1 is equally applicable to the remaining independent claims. Accordingly, claims 11, 21, and 22 should also be in a condition for allowance, as should dependent claims 13, 15-16, 20, and 23.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

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